DUAL PORT MEMORY CORE CELL ARCHITECTURE WITH MATCHED BIT LINE CAPACITANCES

ABSTRACT OF THE DISCLOSURE

A Static Random Access Memory (SRAM) dual port memory with an improved core cell design having internally matched capacitances and decreased bit line capacitance is disclosed. The core cell is fabricated on a substrate divided into three approximately equal columns of different substrate materials. In a preferred embodiment, the memory cell is fabricated on a central p-type column that in turn is sandwiched between two n-type columns. The three-column substrate architecture permits reduced bit line height, with an accompanying reduction in bit line capacitance, which increases the speed at which the core cell can operate. The architecture also permits separating the core cell's bitline and complement bitline, reducing capacitive coupling between these lines and increasing the core cell's operating speed. The architecture further permits better matching of internal node capacitances.